# An Interleaved High-Power Flyback Inverter for Photovoltaic Applications

Bunyamin Tamyurek, *Member, IEEE*, and Bilgehan Kirimer

***Abstract*—This paper presents analysis, design, and implementation of an isolated grid-connected inverter for photovoltaic (PV) applications based on interleaved flyback converter topology operating in discontinuous current mode. In today's PV inverter technology, the simple and the low-cost advantage of the flyback topology is promoted only at very low power as microinverter. Therefore, the primary objective of this study is to design the flyback converter at high power and demonstrate its practicality with good performance as a central-type PV inverter. For this purpose, an inverter system rated at 2 kW is developed by interleaving of only three flyback cells with added benefit of reduced size of passive filtering elements. A simulation model is developed in the piecewise linear electrical circuit simulator. Then, the design is verified and optimized for the best performance based on the simulation results. Finally, a prototype at rated power is built and evaluated under the realistic conditions. The efficiency of the inverter, the total harmonic distortion of the grid current, and the power factor are measured as 90.16%, 4.42%, and 0.998, respectively. Consequently, it is demonstrated that the performance of the proposed system is comparable to the commercial isolated PV inverters in the market, but it may have some cost advantage.**

***Index Terms*—Flyback converter, harmonics, interleaved converters, photovoltaic (PV) inverters.**

## I. Introduction

THE solar energy is considered as one of the most renewable and freely available source of energy and the candidate to play a greater role in the energy market of the world in the near future [1]. Therefore, the research and development in the solar technology field is in the rise [2]–[6], [8]–[20], [22]–[25]. However, the high cost of the technology still limits its usage globally. The low cost is greatly important for commercialization especially in small electric power systems including the residential applications [2]–[6]. Therefore, the primary objective of the study presented in this paper is to contribute to the research and development in the photovoltaic (PV) inverter technology by trying the flyback topology at high power. If it is implemented effectively with good performance, the developed inverter system can be a low-cost alternative to the commercial isolated grid-connected PV inverters in the market.

The simple structure of the flyback topology and easy power flow control with high power quality at the grid interface are the key motivations for this work. The flyback converter is recognized as the lowest cost converter among the isolated topologies since it uses the least number of components. This advantage comes from the ability of the flyback topology combining the energy storage inductor with the transformer. In other type of isolated topologies, the energy storage inductor and the transformer are separate elements. While the inductor is responsible for energy storage, the transformer on the other hand is responsible for energy transfer over a galvanic isolation [7]. The combination of these two components in a flyback topology eliminates the bulky and costly energy storage inductor and therefore leads to a reduction in cost and size of the converter. However, we have to make it clear here that the cost depends on the implementation as much as the selected topology, so not every implementation of the flyback topology leads to a low-cost converter. For this reason, as we try to achieve the high-power implementation of the flyback converter with good performance, which is our primary research contribution, we will also try to preserve the cost advantage during the final implementation step.

Practical implementation of a transformer with relatively large energy storage capability is always a challenge. The air gap is where the energy is stored, so a high-power flyback converter design needs a relatively large air gap. As a result of this, the magnetizing inductance is going to be quite small. The aforementioned challenge is actually achieving such a small magnetizing inductance with low leakage inductance. A flyback converter built with a transformer that has large leakage flux and poor coupling will have poor energy transfer efficiency. Mainly for this reason, the flyback converters are generally not designed for high power. As a result, the flyback topology finds a limited role in PV applications only at very low power as microinverter [10]–[13]. In this technology, every PV panel comes with a dedicated energy conversion unit; a microinverter attached to the output terminals. For this reason, the technology is also named as ac PV module application [14]–[18]. In this practice, many such ac PV modules are connected in parallel to get the desired power output. The maximum harvesting of solar energy in this method is the best since there is a dedicated maximum power point tracker (MPPT) for each PV panel [19]. However, the overall cost of this application is higher compared to the central-type inverter systems.

Nevertheless, when advanced design methods are employed effectively, single-stage flyback converters can be designed and used in high power applications as well. Furthermore, the interleaving of these high-power flyback stages (cells) facilitates developing a central-type PV inverter. The added benefit of interleaving is that the frequency of the ripple components (undesired harmonics) at the waveforms are increased in

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The authors are with the Department of Electrical and Electronics Engineering, Eskisehir Osmangazi University, Eskisehir 26480 Turkey (e-mail: btamyurek@ogu.edu.tr; bilgehankirimer@gmail.com).

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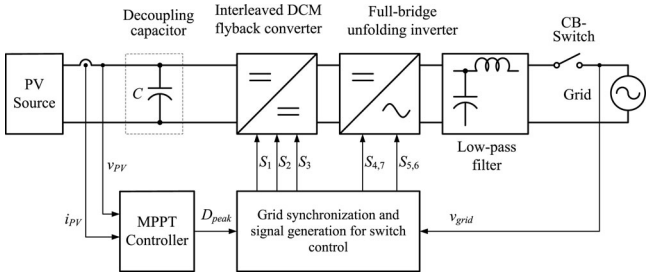


Fig. 1. Block diagram of the proposed grid-connected PV inverter system based on interleaved DCM flyback converter topology.

proportion to the number of interleaved cells. This feature facilitates easy filtering of the ripple components or using smaller sized filtering elements. The ability to reduce the size of passive elements is beneficial for reducing the cost and obtaining a compact converter [21]. Fig. 1 shows the block diagram of the proposed inverter system. The results of an earlier work based on the same topology where the primary objective was to prove the concept with a design at 1 kW were presented in [26]. Since the time of that work, there have been major design changes and upgrades in order to process twice more power and at the same to achieve better overall performance.

As mentioned before, the choice of operation mode for the converter is discontinuous current mode (DCM). The fundamental motivations for selecting DCM operation are summarized as follows.

1) It provides very fast dynamic response and a guaranteed stability for all operating conditions under consideration.
2) No reverse recovery problem. The diodes exhibits reverse recovery problems in CCM operation which cause noise, electromagnetic interference problems, and additional losses. So, DCM operation eliminates all these complications.
3) No turn on losses.
4) Small size of the transformer.
5) Easy control. No need for a feedback loop for the control of the grid current. Only an open-loop control is enough to synthesize a sinusoidal current with good total harmonic distortion (THD). This makes the implementation of the control system less complex for DSP and allows faster execution time.

Contrary to the aforementioned great benefits of the DCM operation, it has several disadvantages as well. In this mode of operation, the current waveforms have higher form factor (high RMS to mean ratio) compared to continuous current mode (CCM). This normally leads to more power losses. So, as a solution, every current carrying path including the switching devices should have low resistivity. Another drawback of DCM operation is the current pulses with large peaks and high amount of discontinuity in the waveforms. Device paralleling is a way to handle the high peak currents. Nevertheless, these disadvantages can be considerably reduced by interleaving of several cells. As a first benefit, the current in each cell will have much less peak but the same amount of discontinuity. However, the discontinuity will be significantly reduced as soon as the cells connect at the common point. All this benefits come from the ability of phase-shifted several cells spreading the power flow evenly over the switching cycle with minimum discontinuity at the source and grid side. In brief, the effective interleaving has the potential to solve or greatly reduce the adverse effects of the DCM operation [21]. Consequently, the circuit diagram of the proposed inverter system based on three-cell interleaved DCM flyback converter topology is shown in Fig. 2.

In conclusion, this study has developed and presented the technology in full detail to produce a grid-tied, isolated, and central-type inverter based on the flyback converter topology at 2 kW, which is not available in today's PV market. The developed system has performed satisfactorily according to major specifications such as the efficiency and the THD of the grid current. Moreover, the study has developed high-power flyback transformers at 700 W and below with extremely low leakage inductance. We also consider this outcome as the significant research contribution since this technology may lead to the development of different applications where the low cost and simplicity are always an issue.

The remainder of this paper is organized as follows. Section II describes the converter topology and defines the operating principles. Section III performs the analysis of the converter and derives the design equations. Section IV presents the design of the converter in steps. Sections V and VI give the simulation and the experimental results, respectively. Finally, Section VII provides the conclusions.

## II. Converter Description and Operating Principles

As shown in Fig. 2, the PV source is applied to a three-cell interleaved flyback converter through a decoupling capacitor. Each flyback converter uses a metal–oxide–semiconductor field-effect transistor (MOSFET) for switching at the primary side, a flyback transformer, and a diode at the secondary side. The topology also has to employ a full-bridge inverter and a low-pass filter for proper interface to the grid. When the flyback switches ($S_1$,$S_2$,$S_3$) are turned ON, a current flows from the common point (the PV source) into the magnetizing inductance of the flyback transformers, and energy is stored in the form of magnetic field. During the on time of the switches, no current flows to the output due to the position of the secondary side diodes; therefore, energy to the grid is supplied by the capacitor $C_f$ and the inductor $L_f$. When the flyback switches are turned OFF, the energy stored in the magnetizing inductances is transferred into the grid in the form of current. So, the flyback inverter acts like a voltage-controlled current source.

The converter is operated in DCM for easy and stable generation of ac currents at the grid interface. The DCM operation of converter under open-loop control produces triangular current pulses at every switching period. If sinusoidal pulse width modulation (PWM) method is used for control, the inverter will regulate these current pulses into a sinusoidal current in phase with the grid voltage [22]. Such currents are shown in Figs. 3 and 4 for a conceptual case. Specifically, Fig. 3 shows the conceptual flyback converter input currents and Fig. 4 shows

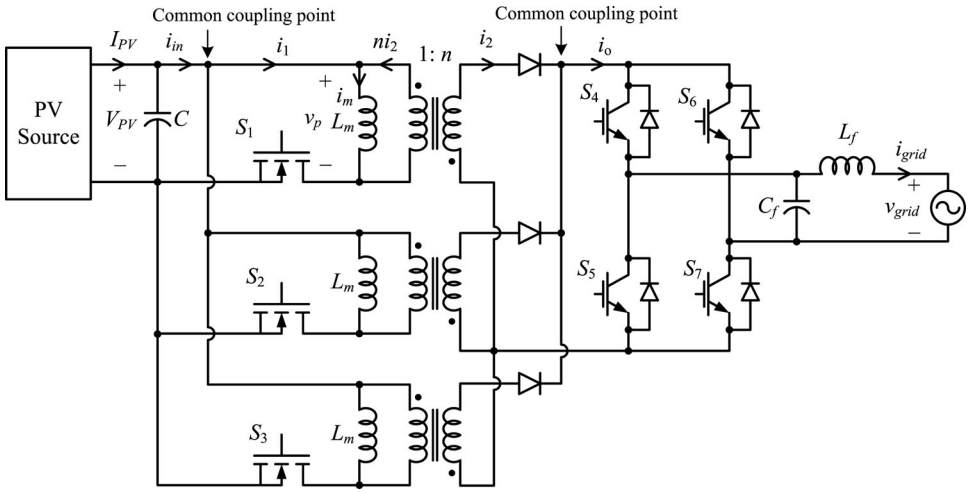


Fig. 2. Circuit schematic of the proposed PV inverter system based on three-cell interleaved flyback converter topology.

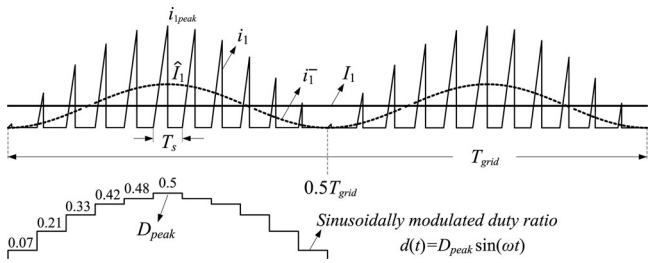


Fig. 3. Instantaneous flyback converter input current ($i_1$), its instantaneous average ($\bar{i}_1$) over one switching period, and the extended average ($I_1$) over one grid period, also the sinusoidally modulated duty ratio over one-half cycle of a grid period.

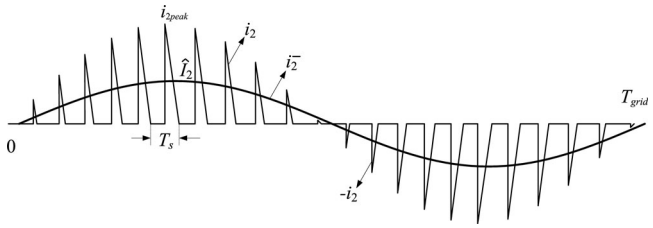


Fig. 4. Instantaneous flyback converter output current ($i_2$) after unfolded by the full-bridge inverter and its instantaneous average ($\bar{i}_2$) over one switching period.

the output currents. As it is seen, the instantaneous currents are composed of discontinuous current pulses with peaks that fall within a sinusoidal envelope since their pulse widths are sinusoidally modulated.

Fig. 3 also shows the three components of the instantaneous flyback converter input current ($i_1$): the high frequency (switching frequency) components, the low frequency (twice the line frequency) component ($\bar{i}_1$) which is the instantaneous average of $i_1$ over one switching period, and the dc component ($I_1$) which is the average over one grid period. In practice, a PV source is not an ideal voltage source; so any ac current that is supplied by it will cause variations at its terminal voltage. So, for good performance of the converter as far as the power utilization and output current distortion, the voltage variations (ripple) across the PV module terminals should be as small as practically possible [20], [23]. For this reason, a decoupling capacitor is placed at the flyback converter input and sized in such a way that both the low and the high frequency ac components are bypassed sufficiently and only the dc (average) component $I_1$ is allowed to be supplied by the PV source. More explanations about this problem and sizing of decoupling capacitor are provided in the analysis section. Fig. 4 shows the instantaneous flyback converter output current ($i_2$) after unfolded by the full-bridge inverter and its instantaneous average ($\bar{i}_2$).

The full-bridge inverter is only responsible for unfolding the sinusoidally modulated dc current packs into ac at the right moment of the grid voltage. Since the switches of the inverter are operated at the grid frequency, the switching losses are insignificant. Only conduction losses are concerned. For this reason, the bridge can use thyristor or even transistor switches for lower cost. However, for easy control also the availability in the laboratory for fast prototyping, we prefer using insulated-gate bipolar transistor (IGBT) switches for this design. But, the final prototype will not use IGBTs. The low-pass filter after the IGBT inverter is responsible for supplying a current to the grid with low THD by removing the high frequency harmonics of the pulsed current waveforms.

## III. Converter Analysis

The analysis of the converter is performed based on the circuit schematic given in Fig. 2 and only considers the first flyback cell. And it is done over one particular switching period when both the grid voltage and the duty ratio are at their peak values. Later, the analysis results will be generalized to include all the cells and extended for the operation of the converter over a full grid period. Consequently, Fig. 5 shows the control signal for the flyback switch, flyback transformer primary voltage ($v_p$), and magnetization current ($i_m$) with its components $i_1$ and $ni_2$ over

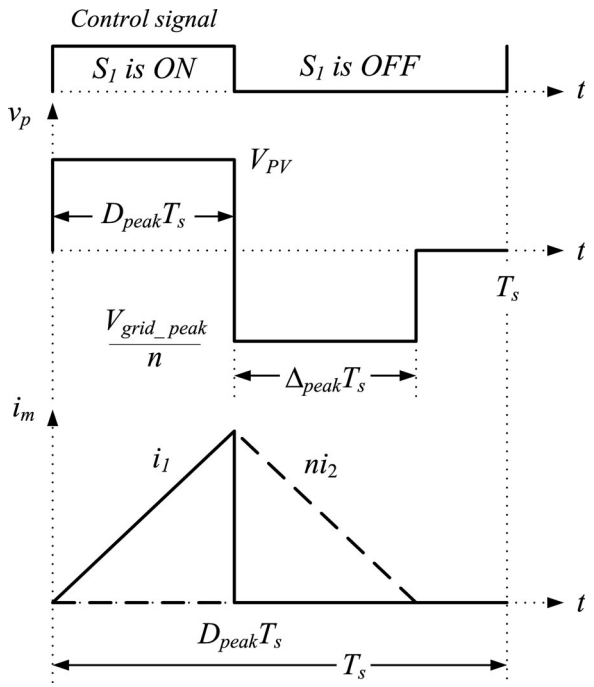


Fig. 5. Flyback switch control signal, flyback transformer primary voltage ($v_p$), and magnetization current ($i_m$) with its components $i_1$ and $ni_2$ over the switching period when the grid voltage is at its peak.

the selected switching period where the duty ratio is at its peak ($D_{\rm peak}$). Note that the waveforms represent DCM operation.

### A. Analysis When the Flyback Switch is Turned ON

When $S_1$ is turned ON in Fig. 2, the PV voltage $V_{\rm PV}$ is applied to the primary winding and a current flows in the primary circuit. The current starts from zero initial value and increases linearly with a positive slope assuming that $V_{\rm PV}$ is constant. The flyback input current (also the magnetizing current) in Fig. 5 can be defined as

$$i_1 = i_m = \frac{V_{\rm PV}}{L_m} t \tag{1}$$

where $L_m$ is the flyback transformer magnetizing inductance. At the end of the switch on time, the current reaches to a peak value as follows:

$$i_{1\rm peak} = i_{\rm mpeak} = \frac{V_{\rm PV} D_{\rm peak}}{L_m f_s} \tag{2}$$

where $f_s$ is the switching frequency. This particular maximum is the peak value of the largest of the sinusoidally modulated triangular current pulses within a half-grid period shown in Fig. 3. The area of this triangle also gives the peak value of the twice the line frequency component of the flyback input current, which is given as follows:

$$\hat{I}_1 = \frac{V_{\rm PV} D_{\rm peak}^2}{2 L_m f_s}. \tag{3}$$

Moreover, the half of this current gives the average (dc) current ($I_1$) that is drawn from the PV source.

$$I_1 = \frac{I_{\rm PV}}{n_{\rm cell}} = \frac{V_{\rm PV} D_{\rm peak}^2}{4 L_m f_s} \tag{4}$$

where $I_{\rm PV}$ is the current delivered by the PV source and $n_{\rm cell}$ is the number of the interleaved cells. Consequently, the relationship between the flyback converter parameters and the PV source output power can be written as follows:

$$P_{\rm PV} = V_{\rm PV} I_{\rm PV} = \frac{n_{\rm cell} V_{\rm PV}^2 D_{\rm peak}^2}{4 L_m f_s}. \tag{5}$$

At the design stage, the desired value of the magnetizing inductance of the flyback transformer ($L_m$) is computed using (5) based on the selected switching frequency, the optimum number of the interleaved cells, and the optimum $D_{\rm peak}$ value. The $D_{\rm peak}$ value is generated by the MPPT controller for maximum harvesting of the solar energy under different irradiation levels and applied to the flyback switches. Note that the entry for $V_{\rm PV}$ in (5) is the PV voltage at MPP.

### B. Analysis When the Flyback Switch is Turned OFF

When $S_1$ is turned OFF in Fig. 2, the flyback transformer primary voltage becomes negative of the grid voltage after scaled by the turn ratio as shown in Fig. 5. The magnetizing current for this case can be written as follows:

$$n i_2 = i_m = \frac{\hat{V}_{\rm grid}}{n L_m} t \tag{6}$$

where $\hat{V}_{\rm grid}$ is the peak of the grid voltage and $n$ is the flyback transformer turn ratio. At the end of the switch off time, the magnetizing current decreases from its maximum value to zero linearly. The change in the current is given as follows:

$$n i_{2\rm peak} = i_{\rm mpeak} = \frac{\hat{V}_{\rm grid} \Delta_{\rm peak}}{n L_m f_s} \tag{7}$$

where $\Delta_{\rm peak}$ is the ratio of the time that takes for the magnetizing current to reset as shown in Fig. 5. It can be computed by equating the Volt–second area across the primary voltage ($v_p$) as follows:

$$\Delta_{\rm peak} = \frac{n V_{\rm PV} D_{\rm peak}}{\hat{V}_{\rm grid}}. \tag{8}$$

Knowing $\Delta_{\rm peak}$ allows finding the peak value of the instantaneous average of the flyback output current ($\bar{i}_2$), which is the area of the largest of the triangular current pulses within a grid period as shown in Fig. 4. Following gives this peak value:

$$\hat{I}_2 = \frac{\hat{I}_{\rm grid}}{n_{\rm cell}} = \frac{V_{\rm PV}^2 D_{\rm peak}^2}{2 L_m f_s \hat{V}_{\rm grid}}. \tag{9}$$

Note that (9) also gives the maximum value of the grid current per interleaved cell. Comparing (5) and (9) verifies the fact that average power from the PV panels equal to the active power

transferred to the grid assuming an ideal converter

$$P_{\mathrm{PV}} = V_{\mathrm{PV}} I_{\mathrm{PV}} = \frac{n_{\mathrm{cell}} V_{\mathrm{PV}}^2 D_{\mathrm{peak}}^2}{4 L_m f_s} = \frac{\hat{V}_{\mathrm{grid}} \hat{I}_{\mathrm{grid}}}{2} = P_{\mathrm{grid}}. \tag{10}$$

In addition, assuming $\Delta_{\mathrm{peak}} = 1 - D_{\mathrm{peak}}$ and using (8), the turn ratio of the flyback transformers can be computed as follows:

$$n = \frac{\hat{V}_{\mathrm{grid}} \left(1 - D_{\mathrm{peak}}\right)}{V_{\mathrm{PV}} D_{\mathrm{peak}}}. \tag{11}$$

The air gap length of the flyback transformer can be found using the following:

$$l_g = \frac{N^2 \mu_0 A_{\mathrm{core}}}{L_m} \tag{12}$$

where $N$ is the number of turns of the primary winding, $\mu_0$ is the permeability of air, and $A_{\mathrm{core}}$ is the cross-sectional area of the core material.

The maximum voltage stress across the flyback switch when it is in off-state can be calculated using the following:

$$V_{\mathrm{SW\,max}} = V_{\mathrm{PV\,max}} + \frac{\hat{V}_{\mathrm{grid\_max}}}{n} + \Delta V \tag{13}$$

where $V_{\mathrm{PV\,max}}$ is the maximum PV voltage, which is actually the open-circuit voltage that may be exist at the input when the inverter is unloaded. $\hat{V}_{\mathrm{grid\_max}}$ is the peak value of the maximum grid voltage. $\Delta V$ is the transient voltage that may occur due to the leakage inductance of the transformer and the parasitic inductances in the circuit during the turn-off of the switch. This transient is generally controlled by a voltage clamp or a snubber circuit. When selecting a switch, it can be taken as the 50% of the nominal switch voltage. In addition, the voltage drop across the secondary-side diodes and the IGBTs are also part of the switch voltage; nevertheless they are more significant in low output voltage applications. They can be ignored in this application because the output voltage is quite high. Finally, the secondary diode faces the maximum voltage stress when flyback switch is ON, and it can be determined as follows:

$$V_{\mathrm{Diode\_max}} = n V_{\mathrm{PV\,max}} + \hat{V}_{\mathrm{grid\_max}}. \tag{14}$$

### C. Analysis for Sizing of Decoupling Capacitor

The control system used in this design does not employ a feedback loop for the regulation of the output current. Therefore, the waveform quality of the grid current is greatly dependent on the quality of the dc voltage at the flyback converter input, which is also the voltage at the PV terminals. For that reason, a relatively constant dc voltage is required for synthesizing a sinusoidal current with low distortion under open-loop control. Otherwise, some low frequency harmonics appears at the grid current causing increased THD. In addition, the ripple at the PV voltage can create slight utilization losses at the PV power as reported in [20]. So, low ripple is also preferred for perfect utilization of the solar power.

The main reason that causes the voltage ripple in single-phase grid-connected PV inverters is the demand of the load by the PV source to deliver fluctuating power with a magnitude twice that of the average power and a frequency twice that of the grid frequency. As explained in Section II, the PV source is not an ideal voltage source, so the terminal voltage is significantly affected by the quality of the current delivered by the module. For that reason, employing a decoupling device is essential to bumper the instantaneous demands from the PV source. The decoupling capacitor works as buffer and provides the power balancing between the PV source and the grid. So, the major sizing criterion of the decoupling capacitor is the effectiveness in diverting the double line frequency component away from the PV source by creating a low impedance path and so maintaining a low ripple at the PV terminals. The following gives the peak-to-peak voltage ripple across the decoupling capacitor

$$\Delta V_{\mathrm{PV}} = \Delta V_C = X_C \Delta I_C \tag{15}$$

where $\Delta V_C$ is the peak-to-peak voltage ripple across, $\Delta I_C$ is the current ripple through, and $X_C = 1/2\pi f C$ is the reactance of the decoupling capacitor. If it is assumed that the entire twice the line frequency (100 Hz) component is bypassed by the decoupling capacitor, then the value of $\Delta I_C$ can be taken as twice the average PV current ($I_{\mathrm{PV}}$). Consequently, using (15), the minimum value of the decoupling capacitor based on the desired peak-to-peak voltage ripple specification can be computed as follows:

$$C \geq \frac{2 I_{\mathrm{PV}}}{(2\pi 100)\, \Delta V_{\mathrm{PV}}}. \tag{16}$$

## IV. Converter Design

Since the design is intended mainly for small electric power systems including residential applications, the power rating is selected as 2 kW. Table I gives the specifications to be used for the design of the proposed inverter system. The switching frequency ($f_s$) is selected as 40 kHz in order to achieve high efficiency along with smaller sized magnetics. In DCM operation, the turn on switching losses are eliminated since the current starts from zero at every switching cycle, which is an important advantage, but in return the switch itself will face large peak current stress and associated high turn-off switching losses. So, the choice of switching device should have fast current fall time ($t_f$) to reduce the turn-off losses. For this reason, we use MOSFET as the flyback switch. Due to the fact that the MOSFETs with low voltage ratings have much lower on-state resistance ($R_{\mathrm{DS(on)}}$) and more efficient as far as the conduction losses are concerned, we prefer low voltage design. As shown in Table I, the maximum converter input voltage is 108.5 V for the selected PV module arrangement. In addition, the flyback switches may face with high voltage stress during turn off due to the leakage inductance of the flyback transformer. So, a clamp and/or a snubber should be employed to keep the switching transients within the safe operating area of the selected devices.

The next important design step is to determine the ideal number of the interleaved cells ($n_{\mathrm{cell}}$). This number is selected as three based on the following strategies.

1) The major objective of interleaving is to reduce the passive filtering efforts to the practical minimum. Thanks to the phase-shifted operation, the ripple (harmonic) magnitude

TABLE I
DESIGN SPECIFICATIONS

| Design parameters | Specifications |
|---|---|
| PV model and maximum power | BP365, 65 W |
| Open circuit voltage and short circuit current per panel | 21.7 V, 3.99 A |
| PV panel group arrangement | 5 panels in a string and 6 strings in parallel |
| Voltage and current at the maximum power point per panel and per the selected panel group arrangement | 17.6 V, 3.6932 A 88 V, 22.16 A |
| Total maximum dc power from the panel group | 1950 W |
| MPPT energy harvesting efficiency | $>98\%$ |
| Inverter static efficiency | $>90\%$ |
| Grid characteristics | Single-phase, 220 V, 50 Hz 143–264 V RMS 45.5–54.5 Hz |
| Grid current percent THD | $<5\%$ |
| Power factor | $>0.99$ |
| Switching frequency | 40 kHz |
| Number of interleaved cells | 3 |

can be reduced while the ripple frequency can be increased simultaneously. So, increasing the number of cells always contributes to the objective. The large cell number is good but then the component count goes up. So, a compromise between the benefit obtained due to the reduced cost and size of the *LC* filters and the disadvantage due to the increased component count must be made.

2) To determine the ideal power rating for the single flyback cell. It is still not very practical to design a single flyback converter at 2 kW at high switching frequency. The efficiency concern puts an upper limit to the power rating. Mainly based on our search at websites of several major component distributers worldwide and also the research reported in the literature recently [27], the commercially available flyback converters in the market are mostly below 200 W. If we go with this general acceptance for a moment, the minimum number of cells to be connected in parallel needs to be 10 in order to reach 2 kW. This means large component count. In this study, however, we propose to achieve the performance of the commercial flyback converters at 700 W, which is mostly guaranteed at low power: 200 W and below. So, this achievement will reduce the cell number from 10 to 3 and yield a moderate increase in the component count while achieving the aforementioned benefits of interleaving. The major modifications to the flyback design at 700 W for good performance are summarized as follows.

a) The flyback transformer will use the most optimum winding strategy for the lowest leakage inductance practically possible. The coils will be tall in height and wide in surface area. The windings will be properly sandwiched and use copper foils. In order to achieve the lowest layer thickness, the windings will use the practical minimum number of turns. Most importantly, the terminal leads that connect the windings to the power circuit will be flat strips that are obtained via proper bending of the copper foils without soldering. In practice, the leads are mostly made using the round conductors soldered to the winding ends. The previous method does not create any space between any parts. Elimination of all the extra space between the turns and the windings except what is required for the insulation significantly minimizes the leakage inductance.

b) Instead of using single component with high current rating, we will use smaller rated components, but put more in parallel to handle the current. Small rated components are cheaper and also contribute to low resistive and low inductive design of the power stage. This modification improves efficiency and reduces the voltage spikes and the associated noise. Moreover, power stage design will use low inductive and resistive paths for connections and use low-inductive screw-type switching devices such SOT227 package.

Based on the selected switching frequency and the cell number, the ripple frequency at the current waveform at the common coupling points (see Fig. 2) becomes 120 kHz. This frequency is high enough for easy filtering of the switching frequency harmonics with relatively small passive elements.

Knowing the cell number yields the information for the duty ratio. It is optimum to select the nominal value of the peak duty ratio as $D_{\mathrm{peak}} = 1/n_{\mathrm{cell}}$. This approach minimizes the discontinuity at the total flyback input current ($i_{\mathrm{in}}$) at the source side. The current waveform obtained under this condition is similar to the operation at the boundary of continuous mode. A duty ratio less than previous criterion results in more discontinuity and larger current peaks. Similarly, a larger duty ratio results in higher waveform peaking due to redundant overlapping of current pulses. The following sections present the design of other units.

### A. Design of PV Stage

In this study, we have used the piecewise linear electrical circuit simulator (PLECS) simulation program for verification of our design work and later for improving its performance. The PLECS software (version 3.5.1) comes with a 65 W PV model developed by the Plexim engineers based on the commercial BP365 part numbered PV panel manufactured by the BP Solar Company. Therefore, for convenience during the simulation studies, we base our design on this PV panel. It is expected that the design should always work with different PV panels

manufactured by different companies as long as the PV voltage and power range are matched. Hence, the PV source selected for the current design uses five BP365 PV panels in a string and six strings in parallel yielding a maximum power of 1950 W at the PV terminals as given in Table I. As mentioned earlier, the experimental setup will use different PV panels with similar characteristics or a PV simulator but provide the same rated output power.

### B. Flyback Transformer Design

The success of the proposed inverter system is very much related to the success in the design and the practical realization of the flyback transformers. As aforementioned, the flyback transformers have to store large amount of energy and then transfer it to the output through magnetic coupling at every switching cycle. Therefore, during the design process, the strategies that first create the most effective energy storage mechanism and second the most optimum and efficient energy transfer path must be employed.

Firstly, the magnetizing inductance of the flyback transformer $L_m$ is determined under nominal conditions. Using 88 V for $V_{\rm PV}$, 40 kHz for $f_s$, 1950 W for $P_{\rm PV}$, 3 for $n_{\rm cell}$, and 0.3333 for $D_{\rm peak}$ in (5), $L_m$ is calculated as 8.27 $\mu$H. Rounding this result to 8 $\mu$H and reworking (5), the practical value of $D_{\rm peak}$ is calculated as 0.3278. Then, the turns ratio of the transformer is determined for the minimum the grid voltage. Using 202 V for $\hat{V}_{\rm grid}$ (minimum peak grid voltage), 88 V for $V_{\rm PV}$, and 0.3278 for $D_{\rm peak}$ in (11), the turns ratio ($n$) is determined as 4.7. But, it is selected as 4.5 for practical implementation. For this design, we selected to use the bar-shaped I93/28/30 part numbered ferrite core with $840$ mm$^2$ cross-sectional area made by Ferroxcube based on 3C94 material. Using $840$ mm$^2$ for $A_{\rm core}$ and 4 for $N$ and 8 $\mu$H for $L_m$ in (12), the air gap length is found as 2.11 mm.

The next major objective in the design of the flyback transformer is to obtain the lowest leakage inductance. This must be achieved for efficient energy transfer to the output. In order to obtain practically the lowest leakage inductance, we have employed the following techniques that are also reported in the recent literature [21].

1) Making the coil and core heights longer so that flux lines can be stretched and forced more into the core, which improves coupling.
2) Reducing the number of winding layers so that less space between the layers. The leakage increases as the number of layers is increased. To reduce layer height, the practically lowest number turns should be used. The low-voltage winding uses four turns and the high-voltage winding uses 18 turns to get the turns ratio of 4.5. The selected number of turns should enable sandwiching of the windings.
3) Using sandwiched windings so that the magnetic field inside the window area is reduced. One level of sandwiching of windings reduces the leakage inductance up to one-fourth compared to the nonsandwiched case [21]. In this application, the low-voltage winding is divided into two halves. Then, the 18 turns of the high-voltage winding is sandwiched between these two halves.

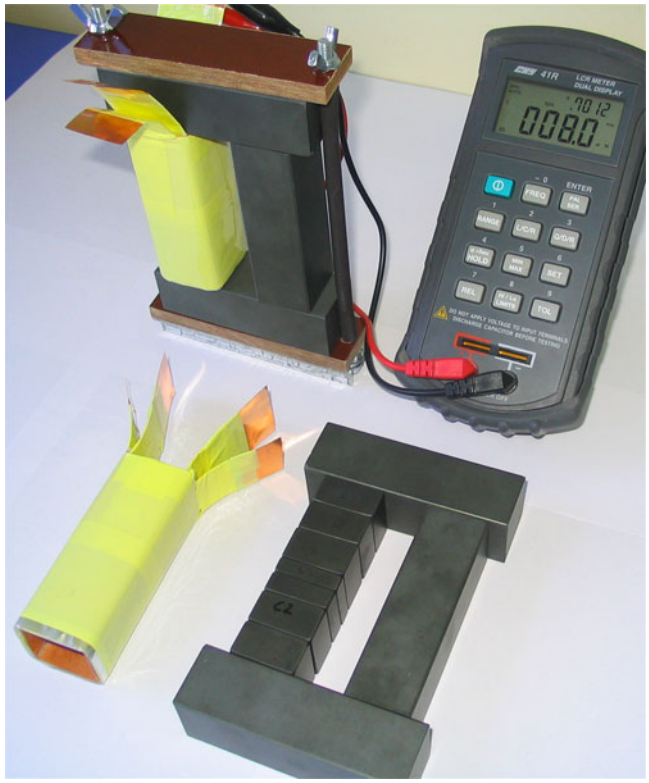

Fig. 6. Flyback transformer constructed for the prototype converter.

4) The terminal leads are made using copper strips with wide surface area instead of round conductors. This method minimizes the parasitic inductance when the high-power flyback transformer is connected to the printed circuit boards. The parasitic inductance would be large if round conductors were used.
5) Distributing of the air gap along the core structure so that fringing flux is minimized. The distributed air gap also contributes to the low leakage by improving the coupling. The air gap length, which is 2.11 mm, is divided into six sections and distributed along one core leg each gap being 0.352 mm as shown in Fig. 6. The top and bottom horizontal bars directly press against the vertical bars without any air gap. So, the major air gap effect is localized in the sliced leg.

The flyback transformer designed and constructed according to previous considerations is shown in Fig. 6. The thickness of the copper foils used for making the windings is selected less than the skin depth requirement at 40 kHz. Also the cross-sectional area of the coppers is more than required. The peak flux density in the core is 0.215 T. The total copper and core losses averaged over a grid cycle are 21.88 W. The magnetizing inductance is 8 $\mu$H and the leakage inductance is less than 0.5%. The constructed transformer is a prototype, so the core structure still needs some size optimization. For example, the length of the top and bottom bars is unnecessarily long as shown in Fig. 6. The final prototype will use the right size of the bars for the optimum size of the core.

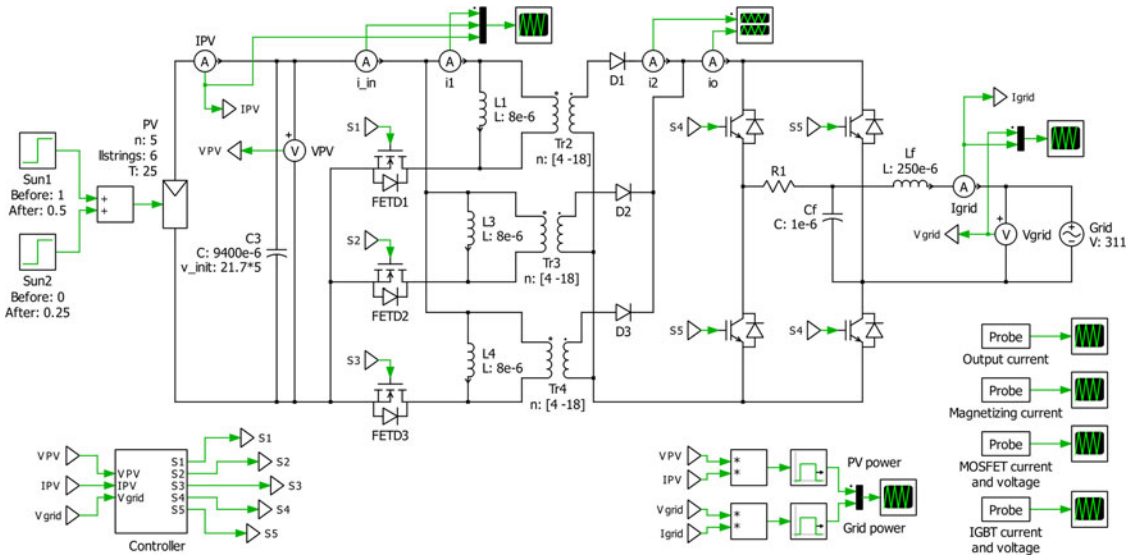


Fig. 7. PLECS model of the proposed PV inverter system including the power stage and the controller.

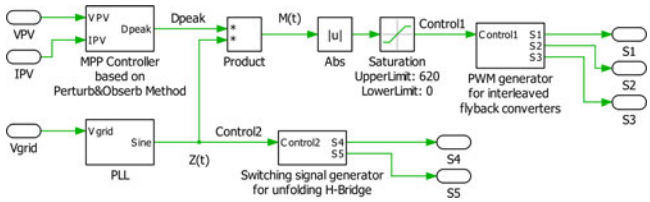


Fig. 8. PLECS model of the control system (inside view of the controller block in Fig. 7).

As a closing remark here, the final air gap length obtained is considered as the second criterion in selecting the optimum power rating for the individual flyback cells. In practice, it is recommended to achieve the final gap length $1/10\text{th}$ less than the side length of the core piece for less flux fringing. For our design, the final gap length is 0.352 mm after the distribution, and the shortest side length is 28 mm, which is already slightly more than the recommended practice. Increasing power further requires smaller magnetizing inductance and a larger air gap length. Then, we should either increase the number of slices in the leg or reduce the number of turns. Reducing the number of turns increase the magnetic flux density which results in higher core losses. Therefore, we consider the current air gap structure as six segments and so the power rating at around 700 W optimum for this design.

### C. PV Inverter Power Stage Design

The decoupling capacitor is an important component of the power stage that controls the voltage ripple at the flyback converter input. As mentioned in the analysis section, smaller the voltage ripple, smaller the THD of the grid current. However, too small ripple means a very large value of capacitance; thus, some compromise must be made between the ripple (correspondingly the THD) and the size. For that reason, a peak-to-peak ripple around 8.5% of the PV voltage at MPP is considered the optimum. This design criterion is determined based on the simulation results that are presented in the following section. According to the simulation results, the 8.5% ripple at the flyback converter input yields 3.9% THD of the grid current, which is considered low enough for the initial design. If the THD somehow turns out to be more than 5% during the experimental verification, the value of the decoupling capacitor is going to be increased until the desired THD is obtained. The percent ripple criterion yields 7.48 V peak-to-peak fluctuation at the inverter input since $V_{\mathrm{PV}}$ is 88 V at MPP. Using 22.14 A for $I_{\mathrm{PV}}$ and 7.48 V for $\Delta V_{\mathrm{PV}}$ in (16), the minimum value of decoupling capacitor is computed as 9422 $\mu$F. Instead of using a large value single capacitor, 20 of 470 $\mu$F 200 V electrolytic capacitors are connected in parallel. Paralleling provides several benefits in this application: it increases the RMS ripple current capability of the capacitor bank; it significantly reduces the equivalent series resistance (ESR) and the equivalent series inductance (ESL). Low value of ESR contributes to the improved efficiency.

Next, the maximum voltage stress across the switching devices should be determined. Based on the given specifications and using 108.5 for $V_{\mathrm{PV}\max}$ 373 V for $\hat{V}_{\mathrm{grid\_max}}$ and 4.5 for $n$ in (13) and (14), the maximum stress across the flyback switch and secondary diodes are calculated as 191.4 V (excluding the transient) and 861.25 V, respectively. If the transient voltage is included, the maximum flyback switch voltage can reach up to 287 V.

The switching frequency of each flyback cell is 40 kHz. Therefore, the ripple frequency of current waveform at the output of the inverter is 120 kHz due to the interleaving. So, the cutoff frequency of the low-pass filter is selected as 10 kHz. Based on the cutoff frequency, the filter elements are selected as $C_f = 1\,\mu$F and $L_f = 250\,\mu$H. Fig. 7 shows the PLECS model (simulation model) of the inverter power stage and the controller used to test and evaluate the performance of the controller and the overall converter design.

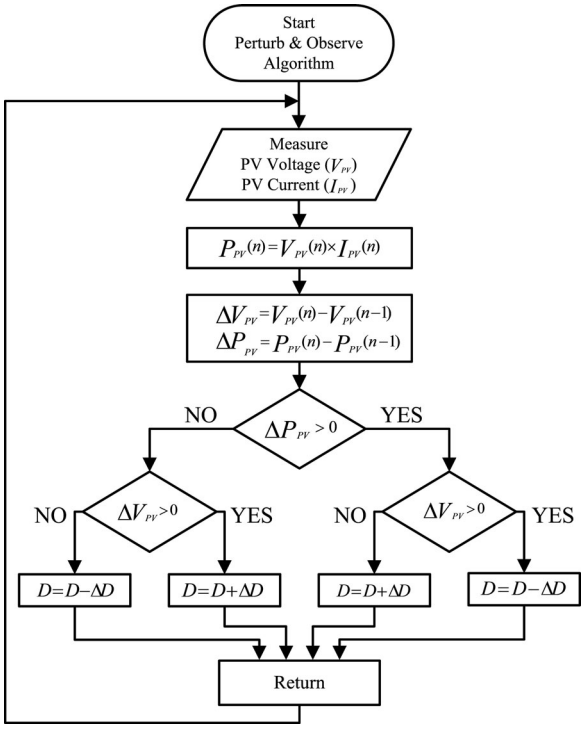


Fig. 9. P&O algorithm implemented in the controller.

The filter capacitor $C_f$ can be placed before the full-bridge inverter contrary to its current location shown in Fig. 7, which may provide two benefits. If the capacitor is placed before the bridge, the ripple current through the IGBTs is the minimum. This can be considered as an advantage for IGBTs in noninterleaved operation. But, it is not a significant advantage in an interleaved operation because the ripple is already reduced. Second, placing the capacitor before the bridge and closer to the secondary diodes reduces the parasitic inductance since the area is minimized. But, using laminated bus bars or PCB for the construction of the output circuit can lower the parasitic inductance. We tried both locations for $C_f$ experimentally and measured no noticeable effect on the operation, performance, and the efficiency of the inverter. In conclusion, one should decide the right place for the capacitor based on his layout preferences. It can be placed at either side of the bridge with insignificant effects on the system.

### D. Control System Design

The control system is designed to perform two important control jobs simultaneously without using a feedback loop. While it is harvesting the maximum power available in the solar cells, it must pump that power into the utility grid with high power quality. For the first job, it should regulate a proper dc current $I_{\rm PV}$ and voltage $V_{\rm PV}$ at the PV interface for maximum energy harvesting. For the second job, it must provide control to convert the dc current, which comes from the panels and continuously regulated for the MPPT purpose, into ac current at the grid interface for power injection. In addition, this ac current should be synchronized with the grid frequency, should have low harmonic distortion, and a power factor close to unity. Fig. 8 shows the details of the control system.

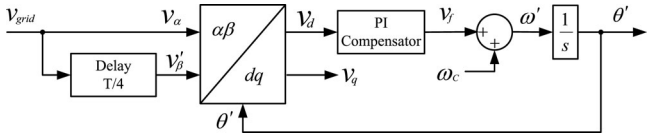


Fig. 10. Implemented PLL structure based on the *T*/4 transport delay technique.

Because of its implementation simplicity, the perturb and observe (P&O) method is selected as the MPPT algorithm [24], [25]. Based on the measured $I_{\rm PV}$ and $V_{\rm PV}$ values, the MPPT block in Fig. 8 generates the peak value of the duty ratio information ($D_{\rm peak}$) in order to regulate the magnitude of the grid current. Similar to the voltage modulation ratio used to regulate the magnitude of the output voltage in a voltage source inverter; the signal generated by the MPPT block in this application regulates the magnitude of the grid current. Fig. 9 shows the flowchart of the P&O algorithm implemented in the DSP controller. The amount of perturbation, which is denoted by $\Delta D$ in the flowchart, is 0.0001.

Besides the magnitude regulation for maximum power transfer, the controller should achieve synchronization of the current with grid voltage and a wave shape that is sinusoidal. For this purpose, the output of the MPPT block is multiplied by the PLL output and the switching signals for the MOSFETs are generated for sinusoidal duty ratio modulation. The PLL output is a sinusoidal waveform with unity gain and synchronized to the grid voltage. The structure of the PLL implemented in this controller is based on the *T*/4 transport delay technique shown in Fig. 10, where *T* is the fundamental period of the grid signal [28].

If this control process is implemented successfully, the instantaneous average of the secondary currents is going to be sinusoidal and in phase with the grid voltage. Another control signal (Control 2) that is also synchronized with the PLL output is used to control the H-bridge IGBT inverter for unfolding purpose. The whole control system is implemented in TMS320F28335 Texas Instrument's DSP Controller. The flowchart of the DSP firmware is illustrated in Fig. 11. In the design of DSP controller firmware, the PWM interrupt is utilized and the controller waits for that interrupt. When the interrupt is generated, all of the processes shown in the flowchart of Fig. 11 are executed and completed in a single PWM interrupt subroutine which takes 25 $\mu$s.

## V. Simulation Results

Before the implementation step, comprehensive simulations are done to verify the design, also to determine some of the hardware requirements. For example, current ratings of the capacitors, inductors, cables, and so on can be easily determined from the simulation results. It is hard to determine RMS ratings by means of only analysis since the current through these elements include several components with different frequencies. Fig. 7 shows the model used during the simulation studies.

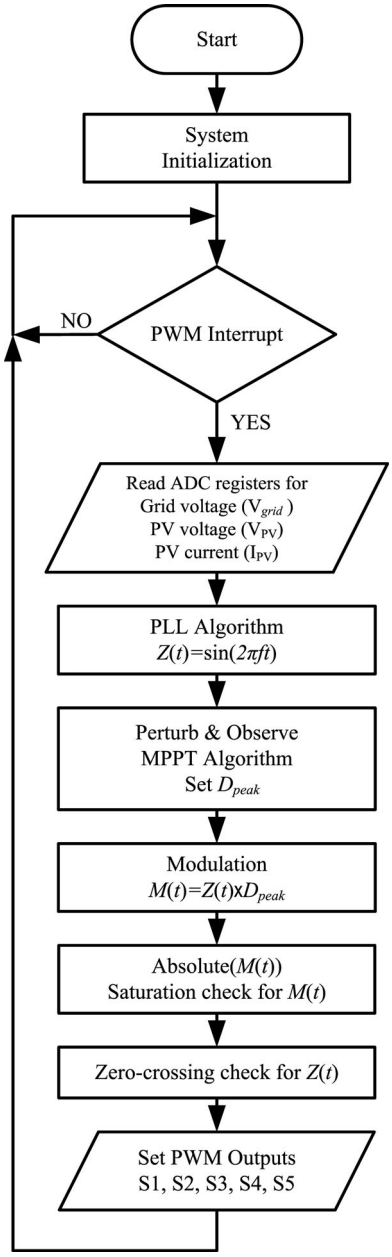


Fig. 11. Flowchart of the DSP firmware implemented in the controller.

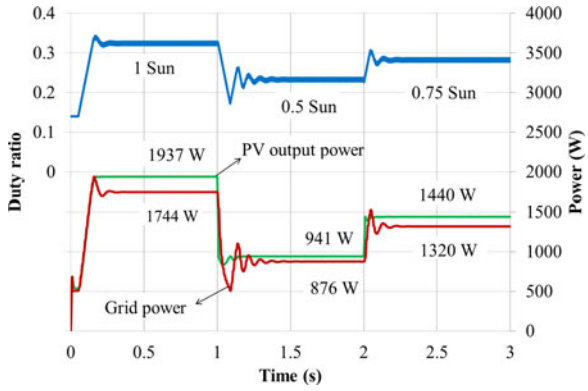


Fig. 12. Peak value of duty ratio generated by the P&O MPPT algorithm for three different Sun levels (top trace), and simulated PV module output power and power delivered to the grid (bottom trace).

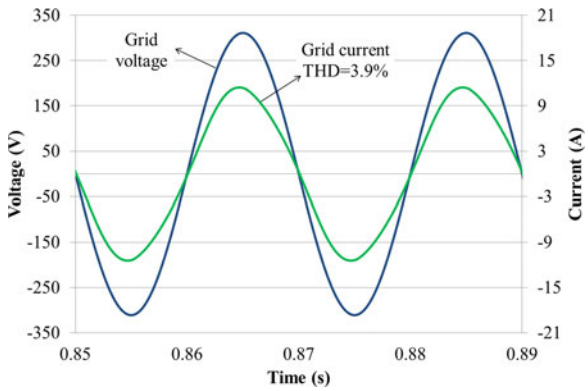


Fig. 13. Simulated waveforms of the grid voltage and current.

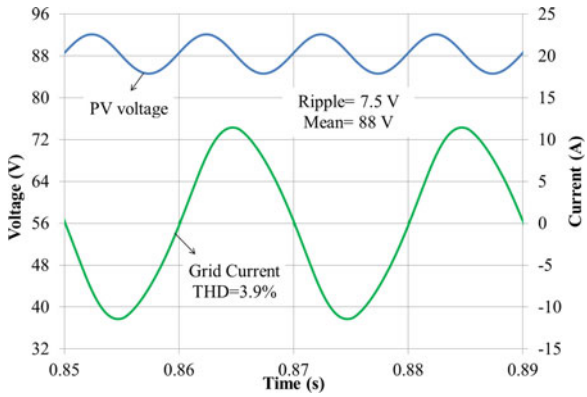


Fig. 14. Simulated waveforms of the PV module terminal voltage and the grid current.

The top trace in Fig. 12 shows the peak value of the duty ratio (also the current modulation ratio) generated by the P&O MPPT algorithm for three different Sun levels; the bottom trace shows the simulated PV module output power and the power delivered to the grid. Based on these results, it can be concluded that the simulated MPPT algorithm works successfully and achieves a tracking performance of 99.33% at the maximum Sun. Moreover, the tracking time is less than 0.1 s. In addition, Fig. 13 shows the simulated waveforms of the grid voltage and current. The waveforms demonstrate the success of the controller and the DCM mode flyback topology in achieving the high quality energy transfer into the grid. Finally, Fig. 14 shows the PV module voltage and the grid current. The top trace indicates 7.5 V peak-to-peak ripple at the PV voltage. The grid current has 3.9% THD under this ripple condition. Moreover, it is verified via simulations that if the value of the decoupling capacitor is increased, the THD reduces almost proportionally. Therefore, if the THD value somehow exceeds the 5% requirement during the experiment, the decoupling capacitor is going to be resized accordingly; otherwise, it is going to be maintained at the selected value.

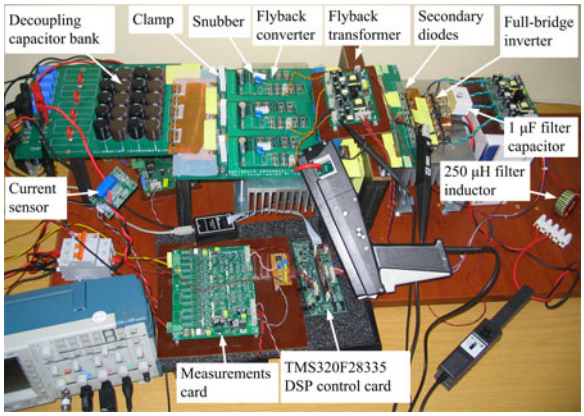


Fig. 15. Experimental setup of the proposed PV inverter system.

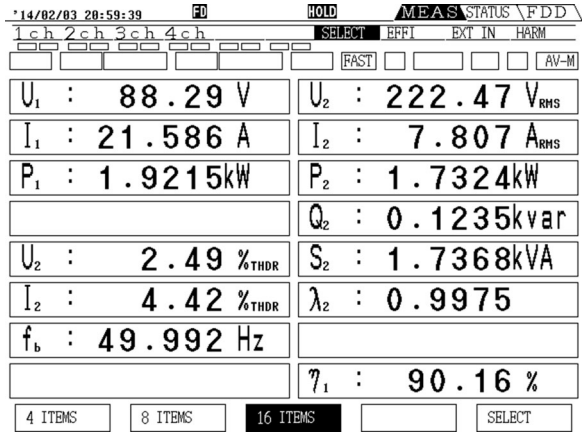


Fig. 16. Experimental results: the screen copy of 3193 Hioki power analyzer.

TABLE II
MAJOR COMPONENTS USED IN THE POWER STAGE

| Part | Description |
|---|---|
| Flyback MOSFET | IXFN80N50P 500 V, 66 A, $\mathrm{RDS(on)} = 0.065$ |
| Flyback diode | APT2×101D120J, 1200 V, 100 A |
| H-bridge IGBTs | APT75GT120JRDQ3, 1200 V, 75 A |
| Decoupling capacitors | 20×(470 $\mu$F, 6.45 A RMS), 169 m$\Omega$/20 Kendeil K05200471_PM0CB |
| Clamp circuit | Clamp resistor: 47 k$\Omega$, 10 W Clamp capacitor: 4.7 $\mu$F, 400 V |
| Snubber circuit | Snubber capacitor: 13 nF Snubber resistor: 66 $\Omega$, 5 W |

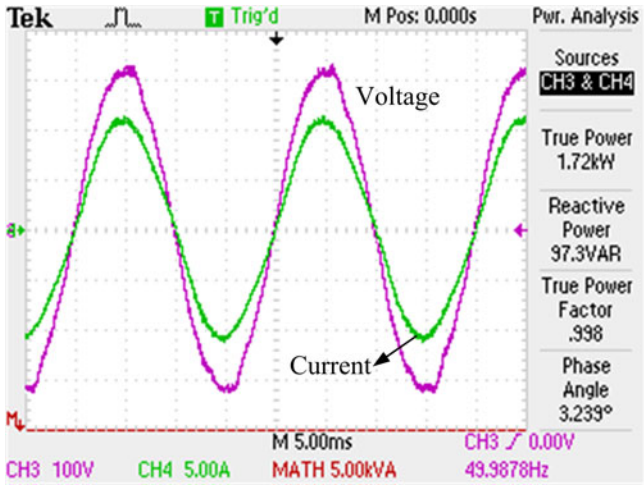


Fig. 17. Experimental waveforms of grid voltage (purple) and grid current (green). Vertical scale: 100 V/div and 5 A/div. Horizontal scale: 5 ms/div.

## VI. EXPERIMENTAL RESULTS

A prototype circuit at rated power was built to evaluate the real-time performance of the proposed inverter system as shown in Fig. 15. The major components used in the prototype circuit are listed in Table II. As seen in Fig. 15, the power stage is constructed using high-quality PCB technology in order to reduce losses and parasitic inductances. The traces on the PCB are made 100 micrometer thick and wide for high RMS current carrying capability. The connections from board to board and from board to transformer terminals are made using copper strips with wide surface area using the laminated bus-bar concept for low inductive and low resistive path. As the final preventive measure to reduce parasitic inductance, the switching components in screw-type SOT227 package are preferred. Even though the setup shown in Fig. 15 is not the final prototype in mind, we did our best to obtain the practically the lowest overall parasitic inductance for this setup, too.

The experimental evaluation of the prototype converter is done using the high accuracy Hioki 3193 power analyzer. Fig. 16 shows the screen view of the measurements taken by this power analyzer. The description of the parameters in the screen is as follows: $U_1$, $I_1$, and $P_1$ are the measured mean PV voltage, current, and power at the maximum power point, respectively; $U_2$ and $I_2$ are the measured RMS grid voltage and current; $P_2$, $Q_2$, and $S_2$ are the grid active, reactive, and apparent powers; $\lambda_2$, $\eta_1$, and $f_b$ are the grid power factor, the inverter static efficiency, and grid frequency, respectively. Finally, $I_{2\%\mathrm{THDR}}$ and $U_{2\%\mathrm{THDR}}$ are the measured percent THD values of the grid current and the voltage, respectively.

The MPPT performance of the inverter is tested higher than 98% for various test conditions with PV modules but at low power. At the proposed power level, however, a dc power supply with a series resistor is used as the PV source since the amount of Sun has not been enough. The dc power supply voltage is set constant at 176 V and the series resistor value at 3.97 $\Omega$ so that the maximum power at the terminals is 1950 W at exactly 88 V. As shown in Fig. 16, the dc power is measured as 1921.5 W, which indicates that the energy harvesting efficiency of the MPPT algorithm at the nominal power is 98.5%.

The grid interface does not require an extra isolation transformer since flyback transformers are providing the desired isolation. Having a good isolation simplifies grid interface allowing a safe wire-to-wire direct connection. However, during testing, the power is not directly injected into grid because of the concerns of weak grid source and harmonics at the grid voltage. Instead, a resistive load with a shunt capacitor is connected to the grid first, and then the converter is operated to supply

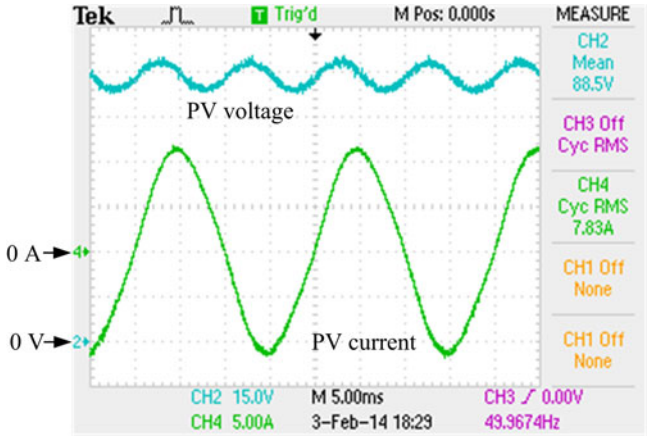


Fig. 18. Experimental waveforms of PV module terminal voltage (blue) and grid current (green). Vertical scale: 15 V/div and 5 A/div. Horizontal scale: 5 ms/div.

TABLE III
POWER LOSSES IN EACH COMPONENT

| Loss parameters | Per flyback cell (W) | Total (W) |
|---|---|---|
| MOSFET turn-off losses | 8.03 | 24.10 |
| MOSFET conduction losses | 20.59 | 61.78 |
| Diode losses | 1.86 | 5.59 |
| Flyback transformer core and copper losses | 21.88 | 65.65 |
| Snubber + clamp losses | 4.48 | 13.45 |
| IGBT conduction losses | | 13.57 |
| Unestimated losses | | 4.98 |
| Total losses | 56.85 | 189.12 |

power to the common point. The value of the shunt capacitor is 3 $\mu$F and is used for filtering of the grid-side noise. As shown in Fig. 16, the power delivered to the load–grid interface is measured as 1732.4 W. The static efficiency of the inverter system is measured as 90.16%. The THD of the grid current and grid voltage is measured as 4.42% and 2.49%, respectively. Finally, the power factor is measured as 0.9975. The results verify the success of the proposed inverter and control system in providing the high power quality output at the grid interface. Moreover, the experimental grid voltage and current measured by the TPS2024 Tektronix oscilloscope shown in Fig. 17 confirm the previous conclusions.

Fig. 18 shows the PV module terminal voltage and the grid current. When it is compared to Fig. 14, the experimental results are very similar to the simulation results. The ripple at the voltage is 7.5 V but the THD of the current is little higher than the simulated value; it is 4.42% instead of 3.9%. Since 4.42% is still less than 5% requirement, the decoupling capacitor is maintained at 9400 $\mu$F. Keeping it at the required minimum is good for our low-cost and the small-size objective.

The measured efficiency of the proposed system (90.16%) is comparable to the two stage schemes where the MPPT stage is generally a boost converter followed by an isolated inverter. The power losses are determined for each component and listed in Table III. According to Table III, the major losses are the

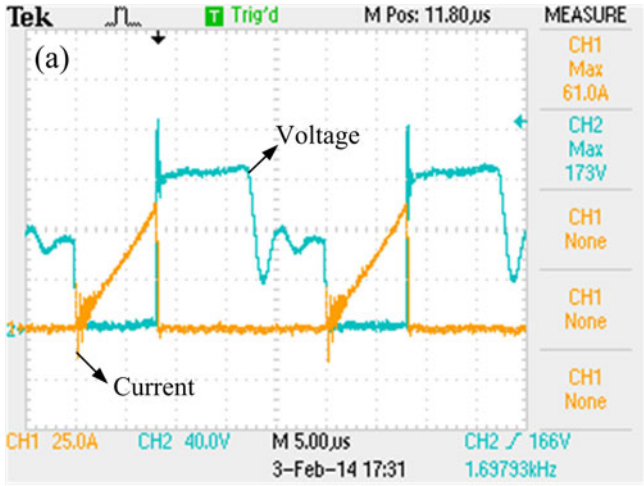


Fig. 19. MOSFET voltage (blue) and current (orange) (a). The closer view of the same waveforms for the worst case (b). Vertical scale: 40 V/div and 25 A/div. Horizontal scales: (a) 5 $\mu$s/div and (b) 250 ns/div.

MOSFET turn-off losses, conduction losses, and the transformer core losses. The losses associated with the MOSFET switch can be reduced using more efficient device such as IXFN132N50P3, which has 500 V rating and has lower RDS(on) (39 m$\Omega$). Using this device lowers the conduction losses to 14.6 W and improves the efficiency to 91.09%. For the low-cost purpose, the soft switching is not employed in this design, but it is the future plan of this project. The performance of the individual flyback cells as far as the efficiency is concerned is slightly better. It is 90.9% with the current MOSFET when the IGBT conduction losses are excluded, and it becomes 91.80% with the suggested MOSFET. This is a good efficiency performance for a flyback converter at 700 W with operation in DCM.

The MOSFET switch voltage and current are shown in Fig. 19. As shown in Fig. 19(b), the peak voltage stress is suppressed at 250 V by using a relatively small RCD snubber at this power level. The snubber circuit uses a 13 nF film type capacitor and a 66 $\Omega$, 5 W resistor. The snubber is combined with a clamp circuit, but the major protection is done by the snubber. Consequently, the ability to handle the voltage stress using 13 nF snubber

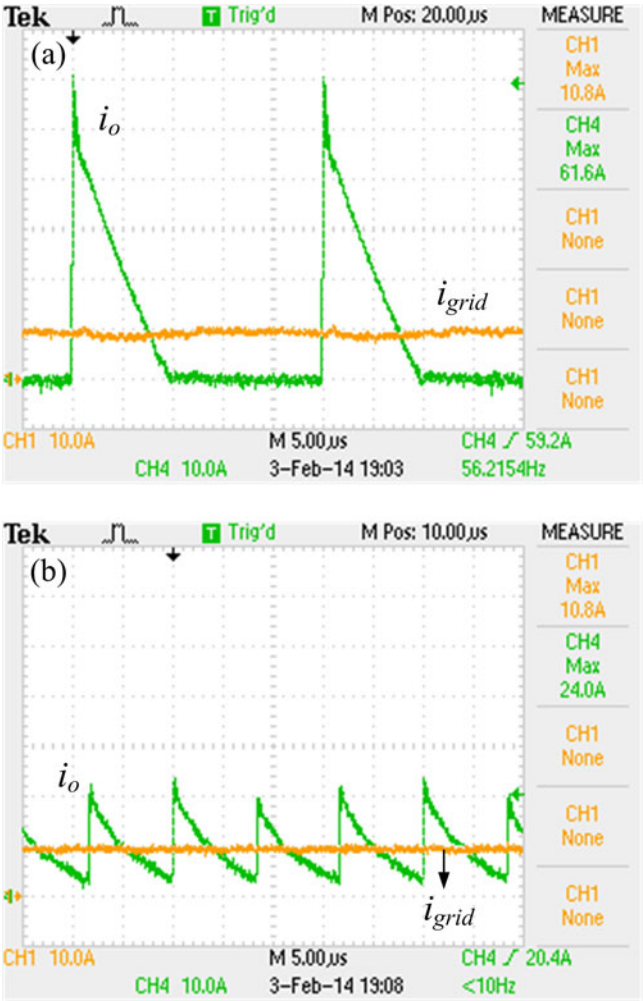


Fig. 20. Measured flyback converter output current (green) and the grid current (orange) for (a) noninterleaved operation. (b) Same waveforms when the interleaved operation is activated. Vertical scale: 10 V/div and 10 A/div. Horizontal scales: 5 $\mu$s/div.

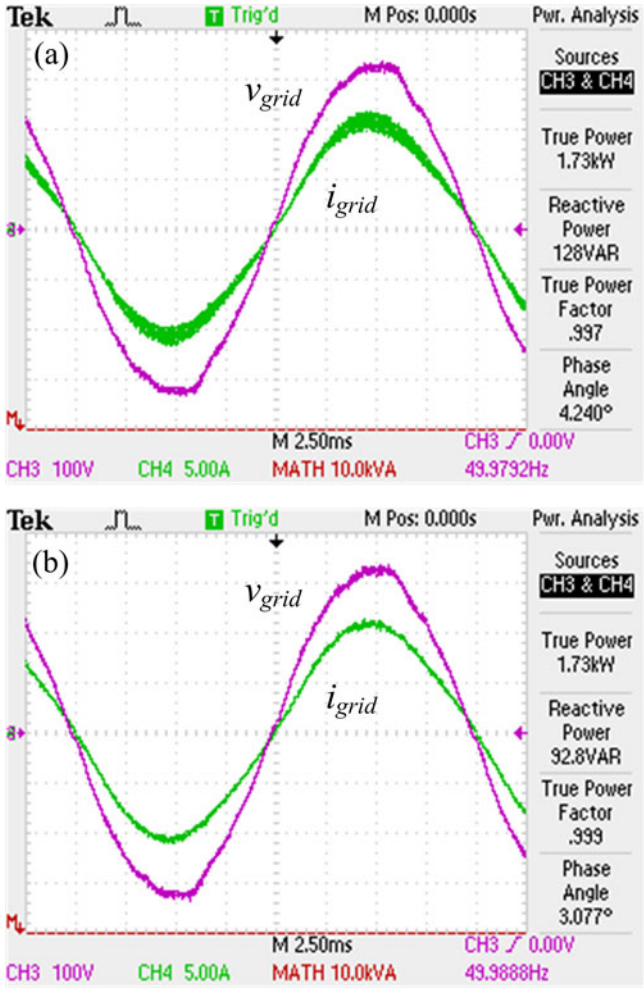


Fig. 21. (a) Grid voltage (purple) and grid current (green) for noninterleaved operation. (b) Same waveforms when the interleaved operation is activated. Vertical scale: 100 V/div and 5 A/div. Horizontal scale: 2.5 ms/div.

capacitance and dissipating less than 5 W in the snubber resistor confirm the low-leakage performance of the flyback transformer.

The test results that demonstrate the benefit of interleaving are shown in Figs. 20 and 21. Fig. 20(a) shows the total output current ($i_o$) after the common coupling point and the grid current for noninterleaved operation. The noninterleaved operation is simulated by putting zero phase shifts among the cells. In this case, the output current before filtering is highly discontinuous and has large peak to average ratio. On the other hand, for the interleaved case, although the individual flyback output currents are still discontinuous, the total output current after common point becomes continuous. The peak current reduces more than half for the same average and the ripple frequency increases and becomes three times the switching frequency as shown in Fig. 20(b). This means that the size of the output *LC* filter especially the size of the filter inductor can be substantially reduced. This reduction in inductor size leads to lowering the cost of the converter. The benefit of interleaving is also clear from the waveforms in Fig. 21. Fig. 21(a) shows the grid voltage and current for the noninterleaved case. The grid current has large ripple in this case. But, in the interleaved case, as seen in Fig. 21(b), the ripple at the current is greatly reduced for the same output filter.

## VII. Conclusion

A central-type PV inverter for small electric power system applications rated at 2 kW is implemented based on the interleaved flyback converter topology. The 2 kW power level is achieved by interleaving of three flyback cells each rated at 700 W. The flyback topology is selected because of its simple structure and easy power flow control with high power quality outputs at the grid interface. The experimental results prove the successful operation of the inverter and compliance to the specifications. The energy harvesting efficiency of the MPPT controller and the inverter static efficiency are measured as 98.5% and 90.16%, respectively. Also, the THD of the grid current is measured as 4.42% and the power factor is 0.998, which are confirming the high power quality interface to the grid. Consequently, it is demonstrated that interleaved flyback topology is practical

at high power as a central-type PV inverter, which is the main contribution of this study. Furthermore, the performance of the proposed system is comparable to the commercial isolated grid-connected PV inverters in the market, but it may have some cost advantage due to its topological benefit.

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**Bunyamin Tamyurek** (M'99) was born in Artvin, Turkey, in 1970. He received the B.S. degree in electrical engineering from Yildiz Technical University, Istanbul, Turkey, in 1991, and the M.S. and Ph.D. degrees in electric power engineering from Rensselaer Polytechnic Institute, Troy, NY, USA, in 1996 and 2001, respectively.

From 2001 to 2003, he was with the American Electric Power, Corporate Technology Development Department, Groveport, OH, where he was involved in the evaluation and testing of the sodium sulfur (NAS) battery systems. While at the AEP Dolan Technology Center, he was a System Expert for the battery and associated interface during the installation of the first U.S. NAS battery energy storage system demonstration project. In 2004, he joined as a Faculty in the Department of Electrical and Electronics Engineering, Eskisehir Osmangazi University, Eskisehir, Turkey. His current research interests include high-power-quality switch-mode rectifiers, energy storage systems, uninterruptible power supply systems, frequency converters, and photovoltaic inverters.

Dr. Tamyurek was an Associate Editor for Letters of the IEEE TRANSACTIONS ON POWER ELECTRONICS between 2006 and 2010.

**Bilgehan Kirimer** was born in Eskisehir, Turkey, in 1989. He received the B.S. degree in electrical and electronics engineering from Eskisehir Osmangazi University, Eskisehir, in 2012, where he is currently working toward the M.S. degree in power electronics area.

His current research interests include photovoltaic inverters and switched mode power supplies.